Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended): A node controller for a node in a data storage system, the node being linked to another node and the nodes being locally coupled to a same host device and a same storage device, ~~having at least two nodes,~~ each node comprising one computer-memory complex and one node controller distinct from said one computer-memory complex, the node controller being operable to transfer data between the ~~two~~ nodes as instructed by a computer-memory complex of the node but without any further intervention by the computer-memory complex, the node controller comprising a cluster memory for storing data being transferred through the node.

Claim 2 (canceled).

Claim 3 (previously presented): The node controller of Claim 28 wherein the at least one data source is one of an interconnect link, a peripheral component interconnect (PCI) bus, or a cluster memory.

Claim 4 (previously presented): The node controller of Claim 28 wherein the logic engine comprises an exclusive OR engine.

Claim 5 (previously presented): The node controller of Claim 28 comprising a command queue operable to store a logic control block to be processed by the logic engine, the logic control block specifying said at least one data source and said at least one data destination.

Claim 6 (original): The node controller of Claim 1 comprising a memory controller operable to interface with a cluster memory in the node.

Claim 7 (original): The node controller of Claim 1 wherein the node controller is implemented as an integrated circuit device.

Claim 8 (original): The node controller of Claim 1 comprising a peripheral component interconnect (PCI) control interface operable to support an interface between the node controller and a PCI bus.

Claim 9 (currently amended): A node controller for a node in a data storage system, the node being linked to another node and the nodes being locally coupled to a same host device and a same storage

device, ~~having at least two nodes,~~ each node comprising one computer-memory complex and one node controller distinct from said one computer-memory complex, the node controller comprising:

a plurality of logic engines each operable to perform a logic operation on non-address data originating from at least one data source in the data storage system and to write a result of the logic operation to a data destination in the data storage system, the logic engine performing the logic operation as instructed by a computer-memory complex of the node but without any further intervention by the computer-memory complex; and

command queues coupled to the logic engines, the command queues operable to store logic control blocks which can be processed by the logic engines.

Claim 10 (original): The node controller of Claim 9 wherein the at least one data source is one of an interconnect link, a peripheral component interconnect (PCI) bus, or a cluster memory.

Claim 11 (previously presented): The node controller of Claim 9 wherein at least one of the logic engines comprises an exclusive OR engine.

Claim 12 (original): The node controller of Claim 9 comprising a memory controller operable to interface with a cluster memory in the node.

Claim 13 (original): The node controller of Claim 9 wherein the node controller is implemented as an integrated circuit device.

Claim 14 (original): The node controller of Claim 9 comprising a peripheral component interconnect (PCI) control interface operable to support an interface between the node controller and a PCI bus managed by the computer-memory complex.

Claim 15 (canceled).

Claim 16 (previously presented): The node controller of Claim 9 comprising:

a producer register operable to specify a first address of a command queue; and

a consumer register operable to specify a second address of a command queue.

Claim 17 (canceled).

Claim 18 (currently amended) A node controller for a node in a data storage system having at least two nodes, each node comprising one computer-memory complex and one node controller distinct from said one computer-memory complex, the node controller comprising:

a memory controller for coupling to (1) a cluster memory and (2) a backplane, wherein the backplane can be coupled to a plurality of other node controllers in the data storage system;

a plurality of input/output interfaces for coupling to a computer-memory complex of the node, a host device, and a storage device all on a plurality of buses ~~and a plurality of devices on a plurality of buses, the plurality of input/output interfaces being coupled to the memory controller~~;

a plurality of logic engines coupled to (1) the memory controller, ~~and~~ (2) the backplane, and (3) the plurality of input/output interfaces;

wherein in a first type of data transfer, one of the logic engines performs a logic operation to a plurality of data from one of a plurality of data sources in the data storage system and writes the result of the logic operation to one of a plurality of data destinations in the data storage system, the data sources comprising the cluster memory and the input/output interfaces, the data destinations comprising the cluster memory, the backplane, and the input/output interfaces.

Claim 19 (previously presented): The node controller of claim 18, wherein in a second type of data transfer, one of the data sources writes a data into the memory and in response one of the logic engines copies the data to at least one of the data destinations.

Claim 20 (canceled).

Claim 21 (currently amended): The node controller of claim ~~20~~ 18, wherein each of the input/output interfaces comprises a peripheral component interconnect (PCI) controller and each of the buses comprises a PCI bus.

Claim 22 (previously presented): The node controller of claim 21, wherein the computer-memory complex manages the PCI bus.

Claim 23 (previously presented): The node controller of claim 22, wherein the computer-memory complex supports a service selected from the group consisting of a HTTP service, a NFS service, and a CIFS service.

Claim 24 (previously presented): The node controller of claim 18, wherein the computer-memory complex is not burdened with temporarily storing data being transferred through the node in the computer-memory complex.

Claim 25 (previously presented): The node controller of claim 18, wherein the logic operation comprises an XOR operation.

Claim 26 (previously presented): The node controller of claim 25, wherein the XOR operation is used to calculate a parity data for writing a full or a partial RAID stripe.

Claim 27 (previously presented): The node controller of claim 25, wherein the XOR operation is used to reconstruct a lost data using a parity data.

Claim 28 (previously presented): The node controller of Claim 1, wherein the node controller comprises a logic engine operable to perform a logic operation on data from at least one data source in the data storage system and to write a result of the logic operation to at least one data destination in the data storage system.

Claim 29 (previously presented): A node controller for a first node in a data storage system comprising at least the first node and a second node, each node comprising one computer-memory complex and one node controller distinct from said one computer-memory complex, the node controller comprising:

a memory controller for accessing a cluster memory of the first node;

one or more bus interfaces for communicating with a host device, a data storage device, and a computer-memory complex of the node all located on one or more buses;

a link to the second node;

wherein in a first type of data transfer:

the computer-memory complex instructs the data storage device to write a data into the memory;

the data storage device writes the data into the memory via the one or more buses;

the computer-memory complex instructs the node controller to send the data to the second node; and

the node controller sends the data to the second node via the link.

Claim 30 (previously presented): The node controller of claim 29, further comprising:

a logic engine;

wherein in a second type of data transfer:

the computer-memory complex instructs the node controller to perform a logic operation to a plurality of data in the memory;

the node controller uses the logic engine to perform the logic operation to the plurality of data.

Claim 31 (previously presented): The node controller of claim 30, wherein the second type of data transfer further comprises:

the computer-memory complex instructs the node controller to send a result of the logic operation to the second node; and

the node controller sends the result to the second node via the link.

Claim 32 (previously presented): The node controller of claim 30, wherein in a third type of data transfer:

the computer-memory complex instructs the data storage device to write the data into the memory;

the data storage device writes the data into the memory via the one or more buses;

the computer-memory complex instructs the host device to read the data from the memory; and

the host device reads the data form the memory via the one or more buses.

Claim 33 (previously presented): The node controller of Claim 9 wherein said at least one destination source is one of an interconnect link, a peripheral component interconnect (PCI) bus, or a cluster memory.

Claim 34 (previously presented): The node controller of Claim 28 wherein said at least one destination source is one of an interconnect link, a peripheral component interconnect (PCI) bus, or a cluster memory.